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... load/ **store** using their last effective **address** and a **...** Predicted loads and **stores** are issued speculatively **...** **Instructions** that depend on **speculative** loads are also **...**
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... Mul- tiple **speculative stores** to the same location create multiple versions **...** If a load is to the same **address** as a **...** can use data bypassed from the **store** when the **...**
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... the thread context with the **address** of the **...** **Speculative** threads must not update the architectural state, for example, by exe- cuting a **store instruction**. **...**
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... commit **speculative** state, and exit **speculative** critical section **...** is elided speculatively, and a future **store** matching the **...** load (ldl_l) to an **address** is followed **...**
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... When a new thread is spawned, the effective **address** of each **store instruction** is predicted as the **...** type of trace, the control flow of **speculative** loop traces **...**
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... To initialize a **speculative** promotion, a spe- cial map **...** the data at the given memory **address** resides in **...** are essentially just special load and **store** operations. **...**
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A comprehensive **instruction** fetch mechanism for a processor supporting **speculative** ...- ▶kfupm.edu.sa [PDF]
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... for a superscalar processor sup- porting **speculative** execution. **...** buffer for the return **instruction** to **store** branch- type **...** the top of the return **address** stack is **...**
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